WEST Search History

DATE: Tuesday, November 25, 2003

Set Name side by side	Query	Hit Count	Set Name result set
DB=JPAB,EPAB,DWPI,TDBD; PLUR=NO; OP=ADJ			
L36	address registers and L35	7	L36
L35	address mode$1	474	L35
L34	operand memories	4	L34
L33	operand address registers	16	L33
DB=USPT,PGPB; PLUR=NO; OP=ADJ			
L32	L31 not L28	30	L32
L31	L29 and L30	32	L31
L30	L25 and decrement$3	34	L30
L29	L25 and increment$3	64	L29
L28	L25 and L27	8	L28
L27	(((711/219)!.CCLS.))	292	L27
L26	L24 and L25	0	L26
L25	(((711/110)!.CCLS.))	157	L25
L24	(((708/672)!.CCLS.))	96	L24
L23	3331056.pn.	1	L23
L22	l18 not L21	150	L22
L21	l18 and L20	14	L21
L20	((711/214)!.CCLS.)	129	L20
L19	L13 and L18	14	L19
L18	(((711/212)!.CCLS.))	164	L18
L17	L13 with bit$1	578	L17
L16	L13 and L15	3	L16
L15	operand address registers	35	L15
L14	L13 same L10	2	L14
L13	address mode$1	2153	L13
L12	L7 same L10	41	L12
L11	L7 and L10	104	L11
L10	4-bit address$2	706	L10
L9	L7 same L8	53	L9
L8	16-bit address$2	1441	L8
L7	8-bit address$2	1273	L7
L6	operand memories	6	L6
L5	multiple operand memories	0	L5
L4	multiple	825693	L4

L3	multiple	825693	L3
L2	L1 same operand memory	4	L2
L1	operand address register	144	L1

END OF SEARCH HISTORY

WEST

End of Result Set

☐ Generate Collection | Print

L2: Entry 4 of 4 File: USPT Mar 10, 1981

US-PAT-NO: 4255785
DOCUMENT-IDENTIFIER: US 4255785 A

TITLE: Microprocessor having instruction fetch and execution overlap

DATE-ISSUED: March 10, 1981

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Chamberlin; George P.	Tempe	AZ		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Motorola, Inc.	Schaumburg	IL			02

APPL-NO: 05/ 946221 [PALM]
DATE FILED: September 25, 1978

INT-CL: [] G06F 9/38

US-CL-ISSUED: 364/200
US-CL-CURRENT: 712/205

FIELD-OF-SEARCH: 364/2MSFile, 364/4MSFile, 364/200, 364/900

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected | Search ALL

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	3462742	August 1969	Miller et al.	364/200
☐	3766527	October 1973	Briley	364/200
☐	3811114	May 1974	Lemay et al.	364/200
☐	3886523	May 1975	Ferguson et al.	364/200
☐	3956738	May 1976	Tessera	364/200
☐	4040031	August 1977	Cassonnet	364/200
☐	4050058	September 1977	Garlic	364/200
☐	4079455	March 1978	Ozga	364/200
☐	4110822	August 1978	Porter et al.	364/200

OTHER PUBLICATIONS

An Introduction to Microcomputers, vol. II, Some Real Products, authored and published by Adam Osborne and Associates, Inc., 1977, pp. 6-18, 6-19.

ART-UNIT: 237

PRIMARY-EXAMINER: Zache; Raulfe B.

ATTY-AGENT-FIRM: Barbee; Joe E.

ABSTRACT:

A microprocessor having separate bidirectional instruction and data busses is disclosed which allows the fetching of instructions from a program memory to be overlapped with the execution of instructions previously fetched. Program instructions are stored in an internal read-only-memory and/or in an external read-only-memory. Variable data is stored in an internal register array. During a given machine cycle, a data word in the register array can be transferred to an arithmetic-logic unit by a bidirectional data bus. The result of the operation performed by the arithmetic-logic unit can be transferred by the data bus back to the register array and stored in the selected location during the same machine cycle. Simultaneously, the contents of a program counter are transferred by a bidirectional instruction memory bus to the program memory to access the instruction to be executed on the following machine cycle. The addressed instruction is transferred from the program memory by the bidirectional instruction memory bus to the microprocessor and is stored to be decoded and executed on the following machine cycle.

7 Claims, 25 Drawing figures

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End of Result Set

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L2: Entry 4 of 4 File: USPT Mar 10, 1981

DOCUMENT-IDENTIFIER: US 4255785 A
TITLE: Microprocessor having instruction fetch and execution overlap

CLAIMS:

1. An integrated circuit data processor capable of executing in an overlapping manner a plurality of macroinstructions stored in a memory in accordance with a plurality of machine cycles, the data processor also being capable of reading data operands from the memory containing the plurality of instructions, comprising:

(a) an address register for storing a first address of a first instruction during a first machine cycle and for storing a second address of a second instruction during a second machine cycle,

(b) an instruction register for storing the first instruction during the second machine cycle and for storing the second instruction during a third machine cycle,

(c) a memory bus coupled to said address register and to said instruction register for transferring the first and second addresses from said address register to the memory, said memory bus also being for transferring the first and second instructions from the memory to said instruction register,

(d) timing means coupled to said address register and to said instruction register for effecting the first, second and third machine cycles,

(e) means coupled to said instruction register and to said timing means for executing the first and second instructions, said means effecting execution of the first instruction during the second machine cycle,

(f) a data operand address register having an output coupled to said memory bus for providing to the memory bus the address of a data operand stored in the memory,

(g) means for storing the data operand addressed by said data operand address register, said storing means having an input coupled to said memory bus for receiving from the memory bus the data operand from the memory, and

(h) a read-only memory coupled to said address register and to said instruction register for storing a plurality of instructions for determining a sequence of operations to be performed by said data processor.

WEST

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L2: Entry 1 of 4 File: USPT Dec 16, 1997

US-PAT-NO: 5699460
DOCUMENT-IDENTIFIER: US 5699460 A

TITLE: Image compression coprocessor with data flow control and multiple processing units

DATE-ISSUED: December 16, 1997

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Kopet; Thomas G.	Colorado Springs	CO		
Taylor; Bradford G.	Colorado Springs	CO		
Lui Kuo; Gerry C.	Colorado Springs	CO		
Lew; Stephen D.	Colorado Springs	CO		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Array Microsystems	Colorado Springs	CO			02
Samsung Electronics Co., Ltd.	Yongin			KR	03

APPL-NO: 08/ 078793 [PALM]
DATE FILED: June 17, 1993

PARENT-CASE:
This application is a continuation-in-part of application Ser. No. 08/054,950, filed Apr. 27, 1993, and now abandoned. Appendix I sets forth descriptions of the instructions used by the coprocessor of this invention.

INT-CL: [06] G06 K 9/46

US-CL-ISSUED: 382/307; 382/232, 364/715.02, 370/85.5
US-CL-CURRENT: 382/307; 382/232, 708/203, 710/107

FIELD-OF-SEARCH: 364/715.02, 364/604, 382/56, 382/232, 382/248, 382/307, 358/433, 370/85.12, 370/85.5

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected Search ALL

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	4651293	March 1987	Kato	364/604
☐	4855813	August 1989	Russell et al.	358/183
☐	4916914	April 1990	Westell	364/604
☐	4985888	January 1991	Madge et al.	370/85.12
☐	5185819	February 1993	Ng et al.	382/56
☐	5212742	May 1993	Normille et al.	382/56
☐	5243667	September 1993	Hirosawa et al.	382/56
☐	5251213	October 1993	Videlock et al.	370/85.12
☐	5267968	December 1993	Coffield	364/604
☐	5388223	February 1995	Guthrie et al.	370/85.5
☐	5475770	December 1995	Mittelbach et al.	382/304

OTHER PUBLICATIONS

Grazia Albanesi "SCPCI: Silicon Compiler Pyramidal Chip for Image Processing" 1989 pp. 191-195.
Smith et al., "Generic ASIC Architecture and Synthesis Schemes for DSP" 1989 pp. 2413-2416.

ART-UNIT: 266

PRIMARY-EXAMINER: Boudreau; Leo

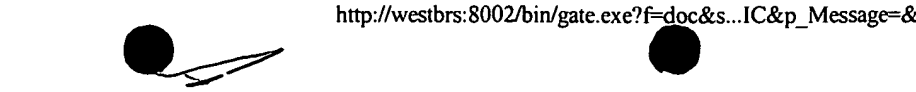
ASSISTANT-EXAMINER: Kelley; Chris

ATTY-AGENT-FIRM: Townsend and Townsend and Crew LLP

ABSTRACT:

The present invention provides an image compression/decompression coprocessor which is integrated on a single chip. The control bus has a control unit which is connected by an internal, global bus to a number of different, special purpose processing units. Each of the processing units is specifically designed to handle only certain steps in compression and decompression processes.

37 Claims, 34 Drawing figures



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L2: Entry 1 of 4 File: USPT Dec 16, 1997

DOCUMENT-IDENTIFIER: US 5699460 A
TITLE: Image compression coprocessor with data flow control and multiple processing units

Detailed Description Text (124):
When ld.sub.-- res.sub.-- pac is asserted and no.sub.-- update is not, Instruction Update Block 1123 loads its "update counter" with the instruction's "number of destinations" field (ND) from the result packet, and starts the update state machine. The process of modifying Operand Memory 821 requires three clock cycles per destination, and each destination is processed in turn. During the first clock cycle, Operand Memory 821 is read at the location selected by the 7 bit "instruction address" portion of the appropriate destination field within the update register, and the fetched 21 bit word is stored in three registers; the 5 bit semaphore field is stored in a "semaphore register", while each of the 8 bit operand address fields is stored in an "operand address register". During the second clock cycle, the most significant bit of the operand address register selected by the 1 bit "operand select" portion of the appropriate update register destination field is set to "1" to indicate "operand present"; the least significant 7 bits of this same register are loaded with the "result address" field from the update register. The semaphore register is loaded with the most significant 5 bits from the update register. During the final clock cycle, the contents of the semaphore register and each of the two operand address registers are written back to Operand Memory 821 at the same location they were read from. The update counter is decremented by "1" each time a destination is processed; when this counter is zero, Instruction Update Block 1123 is deactivated, and Main Controller Block 1121 restarts Instruction Enable Block 1113.

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L15: Entry 28 of 35 File: USPT Feb 19, 1980

US-PAT-NO: 4189768
DOCUMENT-IDENTIFIER: US 4189768 A

TITLE: Operand fetch control improvement

DATE-ISSUED: February 19, 1980

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Liptay; John S.	Rhinebeck	NY		
Rymarczyk; James W.	Poughkeepsie	NY		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
International Business Machines Corporation	Armonk	NY			02

APPL-NO: 05/ 887091 [PALM]
DATE FILED: March 16, 1978

INT-CL: [02] G06F 1/00

US-CL-ISSUED: 364/200
US-CL-CURRENT: 712/204; 712/210

FIELD-OF-SEARCH: 364/2MSFile

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected | Search ALL

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	3496550	February 1970	Schachner	364/200
☐	3569938	March 1971	Eden et al.	364/200
☐	3588829	June 1971	Boland et al.	364/200
☐	3806888	April 1974	Brickman et al.	364/200
☐	3896419	June 1975	Lange et al.	364/200

ART-UNIT: 237

PRIMARY-EXAMINER: Springborn; Harvy E.

ATTY-AGENT-FIRM: Goldman; Bernard M.

ABSTRACT:

Operand controls are provided in an I-unit using address operand pairs (AOPs), each pair consisting of a request register and a buffer register. When handling variable field length (VFL) instructions with source (SRC) and destination (DST) operand addresses, two AOPs are generally assigned to receive different parts of the first subline (e.g. doubleword) of the SRC operand; this is called a duplicate fetch and is used with any size VFL operand. Efficiency is improved for the special case in which the DST operand has all of its bytes confined to a single subline in main storage by detecting the special case and inhibiting a duplicate fetch signal to the I-unit controls which assign duplicate AOPs to an instruction. The SRC operand may have more than one subline but the alignment controls force all source operand bytes into a single subline for the special case. When the duplicate fetch signal is suppressed, only one AOP is assigned by the controls to the first subline fetch for the SRC operand.

3 Claims, 53 Drawing figures

L15: Entry 28 of 35 File: USPT Feb 19, 1980

DOCUMENT-IDENTIFIER: US 4189768 A
TITLE: Operand fetch control improvement

Detailed Description Text (64):
Fig. 2 shows the principle elements making up the operand fetching logic. There are six address register/operand buffer pairs AOP-A through AOP-F, each having a respective one of operand address registers OAR-A through OAR-F and a respective one of operand buffers OP-A through OP-F. The illustrated register pair AOP-A in FIG. 2 shows the operand address register OAR-A associated with the buffer register OP-A, and their controls. The same arrangement is found in each other register pairs AOP-B through AOP-F. A single pair AOP is capable of addressing and receiving a fetch of a doubleword of eight bytes from storage and buffering the received doubleword until its data is needed by E FCT block A15. For each instruction, enough of the six AOP's are assigned so that an entire operand field can be fetched and made available to the execution function as needed.

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L15: Entry 29 of 35 File: USPT Apr 10, 1979

US-PAT-NO: 4149245
DOCUMENT-IDENTIFIER: US 4149245 A

TITLE: High speed store request processing control

DATE-ISSUED: April 10, 1979

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Gannon; Patrick M.	Poughkeepsie	NY		
Sy; Kian-Bon K.	Poughkeepsie	NY		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
International Business Machines Corporation	Armonk	NY			02

APPL-NO: 05/ 805065 [PALM]
DATE FILED: June 9, 1977

INT-CL: [02] G06F 13/06, G06F 9/18

US-CL-ISSUED: 364/200
US-CL-CURRENT: 711/169

FIELD-OF-SEARCH: 364/2MSFile, 364/9MSFile

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected | Search ALL

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	3593314	July 1971	Moll	364/200
☐	3623006	November 1971	Balakian et al.	364/200
☐	4028663	June 1977	Royer et al.	364/900
☐	4070706	January 1978	Scheuneman	364/200

ART-UNIT: 237

PRIMARY-EXAMINER: Nusbaum; Mark E.

ATTY-AGENT-FIRM: Goldman; Bernard M.

ABSTRACT:

The described embodiment provides storage control (PSCF) for overlapping the handling of processor store requests between their generation by an instruction execution means (IPPF) and their presentation to system main storage (MS).

The embodiment uses a store counter, an inpointer counter, an outpointer counter, a translator pointer register, an output counter and a plurality of registers sets to process and control the sequencing of all store requests so that the PSCF can output them to MS in the order received from the IPPF. The embodiment uses the counters to coordinate the varying delays in PSCF processing of plural store request contained in different register sets and the translator.

The store counter obtains independence between plural IPPF operand address (OA) registers which send the store requests and plural PSCF register sets which handle the store request. The number of OA registers is made independent of the number of register sets. The store counter is also used for serializing instruction control.

36 Claims, 15 Drawing figures

L15: Entry 29 of 35 File: USPT Apr 10, 1979

DOCUMENT-IDENTIFIER: US 4149245 A
TITLE: High speed store request processing control

Detailed Description Text (2):
FIGS. 1A-1F illustrate pertinent parts of the circuitry in the processor storage control function (PSCF) containing the subject invention. FIG. 1G illustrates the pertinent circuitry in the instruction preprocessing function (IPPF) interfacing the PSCF circuitry in FIGS. 1A-1F. The store and fetch requests are provided from the IPPF in FIG. 1G on line 10 to line 10 in the PSCF in FIG. 1A. FIG. 1G illustrates the derivation of store and fetch requests from operand address registers OA1 through OAn in the IPPF. Fetch requests are also provided from the instruction fetch control in the IPPF. Each request is presented to PSCF priority circuit 11 in FIG. 1A where it may contend for PSCF bus priority with other storage requests being delayed in the PSCF previously supplied by bus 10 from the IPPF. Contending requests have their processing completed, or partly completed, in the PSCF and are being held by any or more of the four redo registers 16-1, 16-2, 16-3, or 16-4 shown in FIG. 1C or 1D, or in the translator (XL) pointer triggers 14A shown in FIG. 1A. A redo request signal is supplied on line 12, and a translator request signal is supplied on line 13 to PSCF priority circuit 11. Circuit 11 decides which received request is to be put on the PSCF bus by giving highest priority to a translator (XL) request on line 13, next higher priority to a redo store request line 12, and lowest priority to a new store or fetch request from the IPPF on line 10. The IPPF sends only one request at one time.

WEST

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L15: Entry 30 of 35 File: USPT Feb 20, 1979

US-PAT-NO: 4141005
DOCUMENT-IDENTIFIER: US 4141005 A

TITLE: Data format converting apparatus for use in a digital data processor

DATE-ISSUED: February 20, 1979

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Bonner; Bruce R.	Apalachin	NY		
Sliz; Nicholas B.	Apalachin	NY		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
International Business Machines Corporation	Armonk	NY			02

APPL-NO: 05/ 741079 [PALM]
DATE FILED: November 11, 1976

INT-CL: [02] G06F 3/00

US-CL-ISSUED: 340/347DD; 364/200
US-CL-CURRENT: 341/60; 341/89

FIELD-OF-SEARCH: 364/2MSFile, 364/9MSFile, 340/347DD, 235/154

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected | Search ALL

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	3292158	December 1966	Schneberger	364/200
☐	3387280	June 1968	Bina	364/200
☐	3493936	February 1970	Gunderson	364/200
☐	3599186	August 1971	May	364/200
☐	3772654	November 1973	Evans	364/200

ART-UNIT: 236

PRIMARY-EXAMINER: Miller; Charles D.

ATTY-AGENT-FIRM: Bee; Richard E. Seinberg; Saul A.

ABSTRACT:

Data format converting apparatus is described for simultaneously converting multiple bytes of zoned decimal data to packed decimal data or vice versa. In the preferred embodiment, this format converting apparatus is obtained by adding a minimum amount of additional circuitry to a multibyte flow-through type data shifter used for providing the normal data shifting operations in a digital data processor. In particular, a zoned-decimal-to-packed-decimal conversion capability is provided by combining additional switching logic with the normal shifter switching logic for enabling the conductors for nonadjacent data fields on the shifter input data bus to be coupled to the conductors for adjacent data fields on the shifter output data bus. A packed-decimal-to-zoned-decimal conversion capability is provided by adding further switching logic for enabling the conductors for adjacent data fields on the shifter input data bus to be coupled to the conductors for nonadjacent data fields on the shifter output data bus. Control circuitry is provided for selectively enabling either normal data shifting operations or zoned-to-packed format conversion operations or packed-to-zoned format conversion operations. The shifting and format converting hardware is organized so that implementation in the form of large-scale integration circuitry can be accomplished with a minimum number of integrated circuit chips and a minimum number of chip input/output connections per chip.

18 Claims, 41 Drawing figures

WEST

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L15: Entry 30 of 35 File: USPT Feb 20, 1979

DOCUMENT-IDENTIFIER: US 4141005 A
TITLE: Data format converting apparatus for use in a digital data processor

Detailed Description Text (7):
Briefly considering in a general way the procedure for a more or less typical machine language program instruction, the first step is to fetch the instruction from the main storage 17 and to set it into an instruction register 26. This is accomplished by reading the next instruction address from the instruction counter in local store 25 and setting such address into a storage address register (SAR) 27 for the main storage 17. Such address is supplied to SAR 27 by way of a B register 28 and an assembler 29. The addressed instruction is read from main storage 17 and supplied to the instruction register 26 by way of data buses 18 and 13, byte shifter and format converter 14, data buses 15 and 30, destination (D) register 31 and data buses 32 and 33. As part of the instruction fetching operations, the operand addresses are calculated from the base and displacement values contained in the instruction and such results are set into appropriate operand address registers in local store 25. Also, the instruction counter in local store 25 is updated so as to contain the address of the next machine instruction.

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Search Results -

Term	Documents
(18 AND 13).USPT,PGPB.	14
(L13 AND L18).USPT,PGPB.	14

Database: US Patents Full-Text Database; US Pre-Grant Publication Full-Text Database; JPO Abstracts Database; EPO Abstracts Database; Derwent World Patents Index; IBM Technical Disclosure Bulletins

Search: (711/214)!.CCLS. Refine Search

Recall Text Clear

Search History

DATE: Tuesday, November 25, 2003 Printable Copy Create Case

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L19	l13 and L18	14	L19
L18	((711/212)!.CCLS.)	164	L18
L17	l13 with bit$1	578	L17
L16	l13 and L15	3	L16
L15	operand address registers	35	L15
L14	L13 same l10	2	L14
L13	address mode$1	2153	L13
L12	l7 same L10	41	L12
L11	l7 and L10	104	L11
L10	4-bit address$2	706	L10
L9	l7 same L8	53	L9
L8	16-bit address$2	1441	L8
L7	8-bit address$2	1273	L7
L6	operand memories	6	L6
L5	multiple operand memories	0	L5
L4	multiple	825693	L4
L3	multiple	825693	L3
L2	L1 same operand memory	4	L2
L1	operand address register	144	L1

END OF SEARCH HISTORY

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L21: Entry 2 of 14 File: USPT May 27, 2003

US-PAT-NO: 6571330
DOCUMENT-IDENTIFIER: US 6571330 B1

TITLE: Address size and operand size prefix overrides for default sizes defined by an operating mode of a processor

DATE-ISSUED: May 27, 2003

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
McGrath; Kevin J.	Los Gatos	CA		
Clark; Michael T.	Austin	TX		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Advanced Micro Devices, Inc.	Sunnyvale	CA			02

APPL-NO: 09/ 483560 [PALM]
DATE FILED: January 14, 2000

INT-CL: [07] G06 F 9/34, G06 F 9/32, G06 F 9/355, G06 F 12/04

US-CL-ISSUED: 712/210; 712/230, 711/208, 711/209, 711/212, 711/214
US-CL-CURRENT: 712/210; 711/208, 711/209, 711/212, 711/214, 712/230

FIELD-OF-SEARCH: 712/212, 712/227, 712/234, 712/43, 712/213, 712/209, 712/210, 712/230, 711/217, 711/208, 711/209, 711/221, 711/212, 711/214

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected Search ALL

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	4620274	October 1986	Boothroyd et al.	711/217
☐	4701946	October 1987	Oliva et al.	379/102.04
☐	5381537	January 1995	Baum et al.	711/206
☐	5481684	January 1996	Richter et al.	712/212
☐	5517651	May 1996	Huck et al.	712/229
☐	5617554	April 1997	Alpert et al.	711/208
☐	5644755	July 1997	Wooten	703/23
☐	5692167	November 1997	Grochowski et al.	712/226
☐	5758116	May 1998	Lee et al.	712/210
☐	5774686	June 1998	Hammond et al.	712/209
☐	5784638	July 1998	Goetz et al.	712/43
☐	5787495	July 1998	Henry et al.	711/208
☐	5826074	October 1998	Blomgren	712/234
☐	6086623	July 2000	Broome	712/226

OTHER PUBLICATIONS

James L. Turley, "Advanced 80386 Programming Techniques," Osborne McGraw-Hill, 1988, pp. 45-84 and pp. 283-315.
Intel, :Pentium Processor Family Developer's Manual, vol. 3: Architecture and Programming Manual, 1995, pp. 3-1 to 24, 10-1 to 10-13, 11-1 to 11-25.
Pentium.RTM. Pro Family Developer's Manual, vol. 3: Operating System Writer's Guide, .COPYRGT. Intel Corporation 1996, Chapters 2-4, pp. 2-1 through 4-29.
Intel Architecture Software Developer's Manual, vol. 1: Basic Architecture, .COPYRGT. Intel Corporation 1996, 1997, pp. 3-1 through 3-15.

ART-UNIT: 2183

PRIMARY-EXAMINER: Pan; Daniel H.

ATTY-AGENT-FIRM: Merkel; Lawrence J. Meyertons, Hood, Kivlin, Kowert & Goetzel, P.C.

ABSTRACT:

A processor supports a processing mode in which the default address size is greater than 32 bits and the default operand size is 32 bits. The default address size may be nominally indicated as 64 bits, although various embodiments of the processor may implement any address size which exceeds 32 bits, up to and including 64 bits, in the processing mode. The processing mode may be established by placing an enable indication in a control register into an enabled state and by setting a first operating mode indication and a second operating mode indication in a segment descriptor to predefined states. Additionally, an instruction prefix may be coded into an instruction to override the default address and/or operand size. Thus, an address size of 32 bits may be used when desired, and an operand size of 64 bits may be used when desired.

20 Claims, 12 Drawing figures

WEST

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L22: Entry 146 of 150 File: USPT May 22, 1973

US-PAT-NO: 3735355
DOCUMENT-IDENTIFIER: US 3735355 A

TITLE: DIGITAL PROCESSOR HAVING VARIABLE LENGTH ADDRESSING

DATE-ISSUED: May 22, 1973

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Balogh, Jr.; Edward	Diamond Bar	CA		
Cook; Darwen J.	Monroviar	CA		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Burroughs Corporation	Detroit	MI			02

APPL-NO: 05/ 142446 [PALM]
DATE FILED: May 12, 1971

INT-CL: [] G06f 9/20

US-CL-ISSUED: 340/172.5
US-CL-CURRENT: 711/212

FIELD-OF-SEARCH: 340/172.5

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected | Search ALL

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	3470537	September 1969	Goshorn et al.	340/172.5
☐	3422405	January 1969	Packard et al.	340/172.5
☐	3331056	July 1967	Lethin et al.	340/172.5
☐	3400380	September 1968	Packard et al.	340/172.5
☐	3408630	October 1968	Packard et al.	340/172.5
☐	3483526	December 1969	Couleur	340/172.5

ART-UNIT: 237

PRIMARY-EXAMINER: Henon; Paul J.

ASSISTANT-EXAMINER: Vandenburg; John P.

ATTY-AGENT-FIRM: Christie, Parker & Hale

ABSTRACT:

A data processor in which the address fields within the instructions may be of two different lengths in terms of the number of address digits in the field. The number of digits in the address field is determined by the digit in the most significant digit position of the address. If the most significant digit is coded to be a special character, the next six digits are used as the address. If the most significant digit is not coded to be the special character but a decimal digit, it is used together with the next four digits as the address.

10 Claims, 4 Drawing figures

WEST

Generate Collection | Print

L22: Entry 140 of 150 File: USPT Nov 18, 1980

US-PAT-NO: 4234934
DOCUMENT-IDENTIFIER: US 4234934 A

TITLE: Apparatus for scaling memory addresses

DATE-ISSUED: November 18, 1980

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Thorsrud; Lee T.	St. Paul	MN		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Sperry Rand Corporation	New York	NY			02

APPL-NO: 05/ 964994 [PALM]
DATE FILED: November 30, 1978

INT-CL: [] G06F 13/00

US-CL-ISSUED: 364/900
US-CL-CURRENT: 711/212

FIELD-OF-SEARCH: 364/2MS, 364/9MS

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected | Search ALL

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	3681757	August 1972	Allen et al.	364/200
☐	3967251	June 1976	Levine	364/200
☐	4095265	June 1978	Vrba	364/200
☐	4118773	November 1978	Raguin et al.	364/200

OTHER PUBLICATIONS

Crooks et al.-Addressing of Different Size Storage Modules-IBM TDB vol. 17, No. 6-Nov. 1974-pp. 1736-1737.

ART-UNIT: 237

PRIMARY-EXAMINER: Springborn; Harvey E.

ATTY-AGENT-FIRM: Grace; Kenneth G. Cleaver; William E. Truex; Marshall M.

ABSTRACT:

Apparatus for scaling addresses received by a memory module in a modular requestor-memory system in which standard memory modules may be of a discretely variable size and utilized in a plurality of positions in an overall contiguous memory addressing scheme. In particular, this scaling apparatus enables a modular memory which is only partially populated, i.e., only able to respond to a subset of the set of all addresses available, to be located in any one of several positions representing different addressing ranges. This is accomplished without modification of the memory module itself. The memory module knows its discrete capacity, or size, by virtue of the population of the memory array storage locations (array cards) contained therein. The memory module then uses this information to scale, or strip off, the appropriate number of bits from the gross address to allow addressing of the restricted number of memory locations present in the memory module.

5 Claims, 12 Drawing figures

WEST

Generate Collection | Print

L22: Entry 129 of 150 File: USPT Dec 29, 1992

US-PAT-NO: 5175835
DOCUMENT-IDENTIFIER: US 5175835 A

TITLE: Multi-mode DRAM controller

DATE-ISSUED: December 29, 1992

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Beighe; Edward W.	Willow Grove	PA		
Lannutti; Anthony P.	Norristown	PA		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Unisys Corporation	Blue Bell	PA			02

APPL-NO: 07/ 463067 [PALM]
DATE FILED: January 10, 1990

INT-CL: [05] G06F 12/02, G06F 12/00, G06F 12/10

US-CL-ISSUED: 395/425; 364/DIG.1, 364/245.31, 364/400, 365/230.03, 365/230.01
US-CL-CURRENT: 711/212; 365/230.01, 365/230.03, 700/90, 711/105, 711/211

FIELD-OF-SEARCH: 364/245.31, 364/245, 364/245.1, 365/230.01, 365/230.03, 365/230.04, 365/191, 395/425, 395/400

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected | Search ALL

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	4303993	December 1981	Panepinto, Jr. et al.	365/230.03
☐	4346441	August 1982	Plank et al.	364/200
☐	4403283	September 1983	Myntti et al.	364/200
☐	4545010	October 1985	Salas et al.	364/200
☐	4675808	June 1987	Grinn	364/200
☐	4731738	March 1988	Fisher et al.	395/425
☐	4779191	October 1988	Greenblatt	364/200
☐	4805092	February 1989	Cerutti	364/200
☐	4849875	July 1989	Fairman et al.	395/400
☐	4926314	May 1990	Dhuey	364/200
☐	5005157	April 1991	Catlin	365/193
☐	5023777	June 1991	Sawamoto	364/200
☐	5047989	September 1991	Canepa et al.	364/200
☐	5101339	March 1992	Fairman	395/400

ART-UNIT: 232

PRIMARY-EXAMINER: Bowler; Alyssa H.

ATTY-AGENT-FIRM: Sowell; John B. Starr; Mark T.

ABSTRACT:

The present invention provides a novel multi-mode DRAM controller adaptd to access DRAM chips of a main storage unit of different size and of different mode types. The novel DRAM controller comprises new address generation and control logic for delaying the RAS and CAS control signals to memory and for expanding the number of address bits employed to address memory chips having a greater number of addresses by at least one address bit.

7 Claims, 4 Drawing figures

WEST

Generate Collection | Print

L22: Entry 127 of 150 File: USPT May 11, 1993

US-PAT-NO: 5210839
DOCUMENT-IDENTIFIER: US 5210839 A
**** See image for Certificate of Correction ****

TITLE: Method and apparatus for providing a memory address from a computer instruction using a mask register

DATE-ISSUED: May 11, 1993

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Powell; Michael	Palo Alto	CA		
Cmelik; Robert	Sunnyvale	CA		
Kong; Shing	Mountain View	CA		
Ditzel; David	Los Altos Hills	CA		
Kelly; Edmund	San Jose	CA		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Sun Microsystems, Inc.	Mountain View	CA			02

APPL-NO: 07/ 912077 [PALM]
DATE FILED: July 8, 1992

PARENT-CASE:
This is a continuation of application Ser. No. 07/631,967, filed Dec. 21, 1990 now abandoned.

INT-CL: [05] G06F 12/04

US-CL-ISSUED: 395/400; 364/749, 395/775
US-CL-CURRENT: 711/212; 708/518, 711/220

FIELD-OF-SEARCH: 364/2MSFile, 364/9MSFile, 364/736, 364/736.5, 364/748, 364/749, 395/775

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected | Search ALL

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	4199811	April 1980	Borgerson et al.	395/800
☐	4234919	November 1980	Bruce et al.	395/325
☐	4414622	November 1983	Matsumoto	395/400
☐	4521846	June 1985	Scalzi et al.	395/425
☐	4592005	May 1986	Kregness	364/736
☐	4592476	September 1985	Nagafuji	364/749
☐	4729095	March 1988	Culley et al.	395/375
☐	4779195	October 1988	James	395/275
☐	4841438	June 1989	Yoshida et al.	395/800
☐	4945472	July 1990	Sakamura et al.	395/775
☐	4961161	October 1990	Kojima	364/736.5
☐	5074558	December 1991	Bleich et al.	273/121A
☐	5091874	February 1992	Watanabe et al.	364/715.1

OTHER PUBLICATIONS

Shiva, "Computer Design and Architecture", 1985, p. 336.

ART-UNIT: 237

PRIMARY-EXAMINER: Richardson; Robert L.

ASSISTANT-EXAMINER: Barry; Lance Leonard

ATTY-AGENT-FIRM: Blakely Sokoloff Taylor & Zafman

ABSTRACT:

A method and apparatus are provided for enabling a computer that is capable of running programs utilizing different address sizes to run those programs without having to modify the computer's hardware. A mask register is used to identify bits of a sum of register addresses that are valid for the program that is running. The number of valid bits in the register mask can be changed to correspond to the addressable memory size for different programs.

13 Claims, 4 Drawing figures

WEST

Generate Collection | Print

L22: Entry 126 of 150 File: USPT Aug 17, 1993

US-PAT-NO: 5237672
DOCUMENT-IDENTIFIER: US 5237672 A

TITLE: Dynamically adaptable memory controller for various size memories

DATE-ISSUED: August 17, 1993

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Ing-Simmons; Nicholas K.	Bedford			GB2
Robertson; Iain C.	Bedford			GB2

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Texas Instruments Incorporated	Dallas	TX			02

APPL-NO: 07/ 386936 [PALM]
DATE FILED: July 28, 1989

INT-CL: [05] G06F 12/06

US-CL-ISSUED: 395/425; 395/400, 364/DIG.1, 364/243.1, 364/243.7, 364/245.31
US-CL-CURRENT: 711/211; 711/212

FIELD-OF-SEARCH: 395/425, 395/400, 364/9MSFile, 364/2MSFile

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected | Search ALL

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	4234934	November 1980	Thorsrud	395/400
☐	4571676	February 1986	Mantellina et al.	395/425
☐	4649511	March 1987	Gdula	364/900
☐	4675808	June 1987	Grinn et al.	395/400
☐	4744025	May 1988	Lipcon et al.	395/425
☐	4760522	July 1988	Weatherford et al.	395/425
☐	4809234	February 1989	Kuwashiro	365/230.03
☐	4860252	August 1989	Sykora	395/400
☐	4888687	December 1989	Allison et al.	395/425
☐	4908789	March 1990	Blokkum et al.	364/900
☐	4951248	August 1990	Lynch	395/425
☐	4980850	December 1990	Morgan	395/425

OTHER PUBLICATIONS

Mano, "Computer System Architecture", Second edition, 1982, pp. 59-62.

ART-UNIT: 232

PRIMARY-EXAMINER: Dixon; Joseph L.

ASSISTANT-EXAMINER: Nguyen; Hiep T.

ATTY-AGENT-FIRM: Marshall, Jr.; Robert D. Kesterson; James C. Donaldson; Richard L.

ABSTRACT:

There is disclosed a system and method for operating a memory controller in a manner which will allow memories with differing address sizes to be connected to a common bus. The controller decodes address information to change from a determined default address size to another address size on a dynamic basis during the actual memory access cycle. Upon detection of larger memory size, an adjustment occurs in the presentation of address information on the common address bus.

6 Claims, 6 Drawing figures

WEST

Generate Collection | Print

L22: Entry 72 of 150 File: USPT Mar 23, 1999

US-PAT-NO: 5887189
DOCUMENT-IDENTIFIER: US 5887189 A

TITLE: Microcontroller system for performing operations of multiple microcontrollers

DATE-ISSUED: March 23, 1999

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Birns; Neil E.	Milpitas	CA		
Mizrahi-Shalom; Ori K.	San Jose	CA		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Philips Electronics North America Corporation	New York	NY			02

APPL-NO: 08/ 786513 [PALM]
DATE FILED: January 21, 1997

PARENT-CASE:
CROSS REFERENCE TO RELATED APPLICATION This a continuation of application Ser. No. 08/308,774, filed Sep. 19, 1994 now abandoned. This application is related to U.S. applications entitled MICROCONTROLLER WITH A RECONFIGURABLE PROGRAM STATUS WORD by Wang et al., having U.S. Ser. No. 08/308,058, filed Sep. 19, 1994 and issued as U.S. Pat. No. 5,664,156; entitled A PROCESSOR WITH WORD-ALIGNED BRANCH TARGET IN A BYTE-ORIENTED INSTRUCTION SET by Mizrahi-Shalom et al, having U.S. Ser. No. 08/308,337, filed Sep. 16, 1994 U.S. Pat. No. 5,590,358; and entitled METHOD AND APPARATUS FOR FAST MICROCONTROLLER CONTEXT SWITCHING by Birns et al., having U.S. Ser. No. 08/308,770, filed Sep. 19, 1994 now abandoned; all incorporated by reference herein.

INT-CL: [06] G06 F 9/32

US-CL-ISSUED: 595/800.32; 395/800.01, 395/800.36, 711/202, 711/203, 711/212
US-CL-CURRENT: 712/32; 711/202, 711/203, 711/206, 711/209, 711/212, 712/1, 712/36

FIELD-OF-SEARCH: 395/800, 395/800.01, 395/401, 395/427, 395/412, 395/413, 395/421.01, 395/421.07, 395/421.09, 395/421.1, 395/800.32, 395/800.36, 364/DIG.1, 711/262, 711/203, 711/206, 711/209, 711/212

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected | Search ALL

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	4484274	November 1984	Berenbaum et al.	395/678
☐	4495571	January 1985	Staplin, Jr. et al.	395/293
☐	4985848	January 1991	Pfeiffer et al.	395/164
☐	5036458	July 1991	Matsushima et al.	395/591
☐	5050067	September 1991	McLagan et al.	395/678
☐	5062034	October 1991	Bakker	395/500
☐	5159688	October 1992	Matsushima et al.	395/734
☐	5303345	April 1994	Iguchi et al.	395/200.14
☐	5392434	February 1995	Bryant et al.	395/732
☐	5530673	June 1996	Tobita et al.	365/185.09
☐	5649203	July 1997	Sites	395/709
☐	5680600	October 1997	Childers et al.	395/595

FOREIGN PATENT DOCUMENTS

FOREIGN-PAT-NO	PUBN-DATE	COUNTRY	US-CL
0272150	June 1988	EP	
WO94/15287	July 1994	WO	

ART-UNIT: 273

PRIMARY-EXAMINER: Donaghue; Larry D.

ASSISTANT-EXAMINER: Nguyen; Dzung C.

ATTY-AGENT-FIRM: Verdonk; Peter

ABSTRACT:

A microcontroller that provides an environment to run processes developed to run on several prior or low end generation machines with the independent register, status and data space needed for execution, that is, the resources of the microcontroller are a superset of the resources of the prior generation machine. The ability to limit one process from accessing the data space of another independent process is provided by data space segmentation controlled by upper order address bits not accessible by the independent processes. The separate workspaces are configured substantially like a workspace of a prior or low end generation machine allowing the microcontroller to perform the tasks of several independent prior or low end generation machines working in concert.

3 Claims, 7 Drawing figures

WEST

Generate Collection | Print

L22: Entry 47 of 150 File: USPT Mar 6, 2001

US-PAT-NO: 6199155
DOCUMENT-IDENTIFIER: US 6199155 B1

TITLE: Data processor

DATE-ISSUED: March 6, 2001

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Kishida; Takeshi	Osaka			JP
Nakajima; Masaitsu	Osaka			JP

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Matsushita Electric Industrial Co., Ltd.	Osaka			JP	03

APPL-NO: 09/ 267135 [PALM]
DATE FILED: March 11, 1999

FOREIGN-APPL-PRIORITY-DATA:

COUNTRY	APPL-NO	APPL-DATE
JP	10-059680	March 11, 1998
JP	10-115588	April 24, 1998

INT-CL: [07] G06 F 9/30, G06 F 9/34

US-CL-ISSUED: 712/210; 712/218, 711/212, 711/2
US-CL-CURRENT: 712/210; 711/2, 711/212, 712/218

FIELD-OF-SEARCH: 712/210, 712/209, 712/208, 712/211, 712/245, 712/30, 712/42, 712/218, 711/125, 711/119, 711/212, 711/2

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected | Search ALL

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	5440701	August 1995	Matsuzaki et al.	712/210
☐	5845307	December 1998	Prabhu et al.	711/2

FOREIGN PATENT DOCUMENTS

FOREIGN-PAT-NO	PUBN-DATE	COUNTRY	US-CL
0 425 410 A2	May 1991	EP	
0 426 393 A2	May 1991	EP	
0483967	May 1992	EP	
2-293932	May 1990	JP	
WO 97/22924	June 1997	WO	
WO 97/48041	December 1997	WO	

OTHER PUBLICATIONS

Addressing A Second Page of Registers without increasing the Register Field Length, IBM Technical Disclosure Bulletin, vol. 16, No. 3, Aug. 1973 pp. 771-772.
D.R. Ditzel, et al. "The hardware Architecture of the Crisp Microprocessor", The 14th annual International Symposium on Computer Architecture, Jun. 1987, pp. 309-319.

ART-UNIT: 273

PRIMARY-EXAMINER: Pan; Daniel H.

ATTY-AGENT-FIRM: McDermott, Will & Emery

ABSTRACT:

A data processor according to the present invention executes instructions described in first and second instruction formats. The first instruction format defines a register-addressing field of a predetermined size, while the second instruction format defines a register-addressing field of a size larger than that of the register-addressing field defined by the first instruction format. The data processor includes: instruction-type identifier, responsive to an instruction, for identifying the received instruction as being described in the first or second instruction format by the instruction itself; a first register file including a plurality of registers; and a second register file also including a plurality of registers, the number of the registers included in the second register file being larger than that of the registers included in the first register file. If the instruction-type identifier has identified the received instruction as being described in the first instruction format, the data processor executes the instruction using data held in the first register file. On the other hand, if the instruction-type identifier has identified the received instruction as being described in the second instruction format, the data processor executes the instruction using data held in the second register file.

26 Claims, 25 Drawing figures

WEST Search History

DATE: Tuesday, November 25, 2003

Set Name side by side	Query	Hit Count	Set Name result set
DB=USPT,PGPB; PLUR=NO; OP=ADJ			
L22	l18 not L21	150	L22
L21	l18 and L20	14	L21
L20	((711/214)!.CCLS.)	129	L20
L19	L13 and L18	14	L19
L18	(((711/212)!.CCLS.))	164	L18
L17	L13 with bit$1	578	L17
L16	L13 and L15	3	L16
L15	operand address registers	35	L15
L14	L13 same L10	2	L14
L13	address mode$1	2153	L13
L12	L7 same L10	41	L12
L11	L7 and L10	104	L11
L10	4-bit address$2	706	L10
L9	L7 same L8	53	L9
L8	16-bit address$2	1441	L8
L7	8-bit address$2	1273	L7
L6	operand memories	6	L6
L5	multiple operand memories	0	L5
L4	multiple	825693	L4
L3	multiple	825693	L3
L2	L1 same operand memory	4	L2
L1	operand address register	144	L1

END OF SEARCH HISTORY

WEST

End of Result Set

☐ Generate Collection Print

L23: Entry 1 of 1 File: USPT Jul 11, 1967

US-PAT-NO: 3331056
DOCUMENT-IDENTIFIER: US 3331056 A

TITLE: TEXT NOT AVAILABLE

DATE-ISSUED: July 11, 1967

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Name not available				

US-CL-CURRENT: 711/212; 711/171

WEST Search History

DATE: Tuesday, November 25, 2003

Set Name side by side	Query	Hit Count	Set Name result set
DB=USPT,PGPB; PLUR=NO; OP=ADJ			
L23	3331056.pn.	1	L23
L22	l18 not L21	150	L22
L21	l18 and L20	14	L21
L20	((711/214)!.CCLS.)	129	L20
L19	L13 and L18	14	L19
L18	(((711/212)!.CCLS.))	164	L18
L17	L13 with bit$1	578	L17
L16	L13 and L15	3	L16
L15	operand address registers	35	L15
L14	L13 same L10	2	L14
L13	address mode$1	2153	L13
L12	L7 same L10	41	L12
L11	L7 and L10	104	L11
L10	4-bit address$2	706	L10
L9	L7 same L8	53	L9
L8	16-bit address$2	1441	L8
L7	8-bit address$2	1273	L7
L6	operand memories	6	L6
L5	multiple operand memories	0	L5
L4	multiple	825693	L4
L3	multiple	825693	L3
L2	L1 same operand memory	4	L2
L1	operand address register	144	L1

END OF SEARCH HISTORY

WEST Search History

DATE: Tuesday, November 25, 2003

Set Name side by side	Query	Hit Count	Set Name result set
DB=USPT,PGPB; PLUR=NO; OP=ADJ			
L32	L31 not L28	30	L32
L31	L29 and L30	32	L31
L30	L25 and decrement$3	34	L30
L29	L25 and increment$3	64	L29
L28	L25 and L27	8	L28
L27	(((711/219)!.CCLS.))	292	L27
L26	L24 and L25	0	L26
L25	(((711/110)!.CCLS.))	157	L25
L24	(((708/672)!.CCLS.))	96	L24
L23	3331056.pn.	1	L23
L22	l18 not L21	150	L22
L21	l18 and L20	14	L21
L20	((711/214)!.CCLS.)	129	L20
L19	L13 and L18	14	L19
L18	(((711/212)!.CCLS.))	164	L18
L17	L13 with bit$1	578	L17
L16	L13 and L15	3	L16
L15	operand address registers	35	L15
L14	L13 same L10	2	L14
L13	address mode$1	2153	L13
L12	L7 same L10	41	L12
L11	L7 and L10	104	L11
L10	4-bit address$2	706	L10
L9	L7 same L8	53	L9
L8	16-bit address$2	1441	L8
L7	8-bit address$2	1273	L7
L6	operand memories	6	L6
L5	multiple operand memories	0	L5
L4	multiple	825693	L4
L3	multiple	825693	L3
L2	L1 same operand memory	4	L2
L1	operand address register	144	L1

END OF SEARCH HISTORY

L33: Entry 9 of 16 File: TDBD Apr 1, 1982

TDB-ACC-NO: NA82045410

DISCLOSURE TITLE: Creation of Super Instructions In Hardware. April 1982.

PUBLICATION-DATA:
IBM Technical Disclosure Bulletin, April 1982, US

VOLUME NUMBER: 24
ISSUE NUMBER: 11A
PAGE NUMBER: 5410 - 5414

PUBLICATION-DATE: April 1, 1982 (19820401)

CROSS REFERENCE: 0018-8689-24-11A-5410

DISCLOSURE TEXT:

5p. High performance processors like the IBM System/370 Model 3033 use a hardwired instruction preprocessing function unit (IPPE) and microcoded execution (E) unit. An ideal instruction goes through the pipelined lined machine in four cycles as follows: In the first cycle (D/A), the instruction is decoded to determine the needs in terms of general purpose registers (GPRs) and operands from cache, and information relevant to its execution activity is placed in a four-position queue between the IPPF and the E unit. In the next cycle (C1), the operand access for the instruction if any is begun. In the third cycle (C2), the operand arrives from the cache (assuming a hit in the cache) while the micro-instruction to execute the instruction is read out of control storage and the working registers in the E unit are set up in preparation of the execution of the instruction. The instruction is executed in the next cycle (E), and the results are put away in the follwing cycle. - In general, instructions processed by the CPU are dependent on each other. The design of both the instruction (I) unit and the E unit implicitly recognizes such dependence to speed up the processing of instructions. The Load Bypass is an example of such a mechanism in the I unit, while the Wrap to A register and Wrap to B register serve a similar purpose in the E Unit. - The purpose here is to disclose a mechanism that explicitly recognizes when certain frequent, mutually dependent instructions are processed by the I unit, creates a 'super instruction' that does the same work as the instruction sequence it replaces, and executes the super instruction in the E unit in a fewer number of cycles than the original instruction sequence. For some pairs this is accomplished without changes in the E unit except for changes in microcode. - There is no change in the sequence or number of instructions processed by the I unit or the number of cycles taken by the I unit. For some pairs there is no change in the total amount of work done by the E unit or the sequence in which it is done (except that it is done in fewer cycles). Thus, there should be no problems with architecture specified orders or instruction retry. - The concept is illustrated below in the context of a frequent pair of instructions: (TM, BC(R)), where TM is Test under Mask and BC is Branch on Condition, though it will work equally well for (CLI BC(R)), (LTR BC(R)), and other pairs. :BC is decoded, then a super-instruction can replace the instruction sequence (TM, BC). This is done by reading out a micro-instruction(s) that corresponds to the super-instruction rather than just the TM. The :BC Successful signal is generated during the execution cycle of the TM instruction (early generation of BC Successful); thus, the execution cycle of the BC is a null cycle. Thus, in this case the super-instruction corresponds to a micro-instruction sequence that does the work currently being done for TM; the execution cycle activity for BC, having been done during the execution cycle of TM, is eliminated. - The concept of super-instruction is

described in greater depth below and specific implementation is provided. The loop in Fig. 1 occurs frequently in scientific/ engineering applications. One possible execution is shown in Fig. 2 (D, A, C, E, P, B refer respectively to Decode, Address generation, Cache access, Execute, Putaway and BXLE preexecution in the I Unit). - Even with the reduced E times, the multiply-add loop is still E unit limited. A further improvement in E time is obtained by eliminating the separate LD cycle in the E unit. This is accomplished as follows: If the I unit, on successive cycles, decodes the two instructions: LD 0,X MD 0,Y It creates a new super-instruction MD' 0, FLB1, FLB2. This instruction is written over the LD instruction in the queue between the I and E units. A new microstore address is provided and during set-up, FLB1 and FLB2 are gated to A and B. The multiply proceeds as usual with the result going to floating point register 0. The same scheme can be used with additional pairs, such as (LD, AD), (LD, SD), etc. - A typical timing sequence with the LD overlap is shown in Fig. 3. An LD is decoded in cycle 7 and placed in the queue. This location would normally not be active until cycle 13. During cycle 8, MD is decoded and the potential for a super-instruction is recognized. The earlier LD information in the queue is replaced by MD'. In cycle 13, a new micro-instruction is read out and the I unit causes the transfers FLB1 approaches A and FLB2 approaches B. (Two Op buffer copies are therefore require It should be noted that by cycle 11 the operands are actually available in the E unit. The multiplication continues from cycle 14 to 18 under control of a new micro-routine. - A single set of six operand buffers can be utilized in one to one relation with the six operand address registers. The buffers are loaded from the cache bus. During staging, the I unit can gate the operand buffers to either the A or the B staging registers. The proposed super-instruction scheme is shown in Fig. 4, and the buffers are loaded simultaneously. Copy 1 of the buffers goes to A-reg and cpu 2 tp Breg. The I unit uses appropriate control lines to activate the transfers FLB1 approaches A and FLB2 approaches B in parallel. Once the hardware penalty is paid, various pairs of instructions can be handled with only micro-store impact. - The advantages are as follows: 1. Significant performance improvement for sample loops. 2. No software impact. 3. Maintains one at a time execution philosophy. Exception handling/Instruction retry handled by new micro-routine. - (If necessary the pair can be reexecuted sequentially, i.e., with the super-instruction feature switched off.) 4. Once the hardware penalty is paid, very little penalty for additional super-instructions.

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L33: Entry 16 of 16 File: DWPI Aug 5, 1975

DERWENT-ACC-NO: 1976-D2156X
DERWENT-WEEK: 197614

TITLE: Simplified control for programmed data processor - combines functions of structural circuits in others by distributor

PATENT-ASSIGNEE: LENGD KALININ POLY (LEKA)

PRIORITY-DATA: 1972SU-1771715 (April 17, 1972)

PATENT-FAMILY:

PUB-NO	PUB-DATE	LANGUAGE	PAGES	MAIN-IPC
SU 478307 A	August 5, 1975		000	

INT-CL (IPC): G06F 9/06

ABSTRACTED-PUB-NO: SU 478307A
BASIC-ABSTRACT:

This invention concerns computer technology and can be used for controlling the operation of a programmed specialized digital computer, or for implementing standard subprogrammes in general-purpose digital computers. Simplifications are proposed on grounds of economy. Essentially, in the proposed device each output of a distributer (1) is connected to the corresponding recording inputs of an operand address decoder (5), operand address registers (3, 4), operation code decoder (6), and instruction address registers (7, 8). The circuitry also includes output rails (2), outputs (9-18), inputs (19, 20), and the diode matrices (21-28). As a result the device no longer requires a permanent storage device, and there is a saving of one operand address register and one operation code register. If the circuitry is based on logical elements, there is an advantage in using magnetic switches which have perforated cores.

ABSTRACTED-PUB-NO: SU 478307A
EQUIVALENT-ABSTRACTS:

DERWENT-CLASS: T01

Print Request Result(s)

Printer Name: cpk2_2b02_gbgiptr
Printer Location: cpk2__2b02

- SU000478307A: At least one of the requested patents was not found

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L34: Entry 4 of 4 File: DWPI Nov 7, 1986

DERWENT-ACC-NO: 1987-183780
DERWENT-WEEK: 198726

TITLE: Variable-length computer operands pre-processor - has operand attribute inputs to byte address subtraction control circuit for byte address subtractors at inputs to corresp. memories

INVENTOR: LOPATO, G P; PODGORNOV, A I ; ZAPOLSKII, A P

PATENT-ASSIGNEE: LOPACO G P (LOPAI)

PRIORITY-DATA: 1984SU-3719951 (April 6, 1984)

PATENT-FAMILY:

PUB-NO	PUB-DATE	LANGUAGE	PAGES	MAIN-IPC
SU 1269147 A	November 7, 1986		008	

APPLICATION-DATA:

PUB-NO	APPL-DATE	APPL-NO	DESCRIPTOR
SU 1269147A	April 6, 1984	1984SU-3719951	

INT-CL (IPC): G06F 13/00; G06F 15/20

ABSTRACTED-PUB-NO: SU 1269147A
BASIC-ABSTRACT:

The circuitry contg. a register (1) at the data input (2), operand memories (3,4), mask coders (7,8) and the operand length code input (9), has a clearing input to the OR-gate (10), AND-gates (11,14), NOT-gate (13), sync input (15), trigger (16), a byte address subtraction control circuit (18), byte address subtractors (19,20), multiplexers (24,25) and the decoders (26,27).

Initially the value of two LSB digits of the external memory addresses for each operand are entered in the input register. In performing e.g. the operation of decimal addition, the first operand may be 12 bytes in length and have 10 as the external memory address; the other operand can be seven bytes in length and have the address 01. The byte address subtraction control circuit indicates the byte in a work from the local memory address of which it is necessary to subtract 1. The byte address subtractors modify the byte address of the first and second operands by subtraction of 1 on address to the memory. Data of variable length can be arranged in integer boundaries of words.

USE/ADVANTAGE - In processors of medium and high productivity computers, operating speed is increased in pre-processing of variable-length operands. Bul.41/7.11.86

ABSTRACTED-PUB-NO: SU 1269147A
EQUIVALENT-ABSTRACTS:

CHOSEN-DRAWING: Dwg.1/5

DERWENT-CLASS: T01
EPI-CODES: T01-J;

Print Request Result(s)

Printer Name: cpk2_2b02_gbgiptr
Printer Location: cpk2__2b02

- SU001269147A: At least one of the requested patents was not found

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L36: Entry 4 of 7 File: DWPI Jan 18, 2001

DERWENT-ACC-NO: 2001-464524
DERWENT-WEEK: 200263

TITLE: Indirect access provision apparatus for very long instruction word processor, selects very long instruction word in very long instruction word instruction memory using address generating mechanism

INVENTOR: BARRY, E F; PECHANEK, G G

PATENT-ASSIGNEE: BOPS INC (BOPSN)

PRIORITY-DATA: 1999US-0350191 (July 9, 1999)

PATENT-FAMILY:

PUB-NO	PUB-DATE	LANGUAGE	PAGES	MAIN-IPC
WO 200104765 A1	January 18, 2001	E	041	G06F015/00

DESIGNATED-STATES: CA IL JP KR AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE

APPLICATION-DATA:

PUB-NO	APPL-DATE	APPL-NO	DESCRIPTOR
WO 200104765A1	June 7, 2000	2000WO-US40143	

INT-CL (IPC): G06 F 12/00; G06 F 15/00

RELATED-ACC-NO: 2002-461659;2002-582970

ABSTRACTED-PUB-NO: WO 200104765A
BASIC-ABSTRACT:

NOVELTY - The apparatus includes a short instruction memory (SIM) (105), SIM fetch logic (103), instruction decoder, very long instruction word (VLIW) instruction memory (VIM) (109), VLIW memory address unit (VIM AGU) and associated VIM address registers. A VIM address generation mechanism selects a VLIW in a VIM by generating a VIM address.

DETAILED DESCRIPTION - The apparatus includes an instruction register for storing an instruction including direct address bits. The VIM AGU determines if the instruction in the instruction register is a direct VIM addressing mode instruction and provides direct addressing mode control signals to the VIM address generation mechanism. INDEPENDENT CLAIMS are also included for the following:

(a) Base plus index addressing mode apparatus;

(b) Circular indexed addressing mode apparatus;

(c) Processing element providing method;

(d) Processing element selective execution method;

(e) Synchronous MIMD operation providing method

USE - For instruction addressing in indirect very long instruction word processor in signal processing application.

ADVANTAGE - Allows for greater flexibility in opcode space making more bits available by the use of register based address modes. Allows synchronous MIMD mechanism for selection of different VLIW in each processing element in parallel.

DESCRIPTION OF DRAWING(S) - The figure illustrates 2 multiply 2 VLIW processor.

ABSTRACTED-PUB-NO: WO 200104765A
EQUIVALENT-ABSTRACTS:

CHOSEN-DRAWING: Dwg.1/8

DERWENT-CLASS: T01
EPI-CODES: T01-H; T01-J;